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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.**	**Applicant(s)**	
	10/681,860	CROSLAND ET AL.	
	Examiner	**Art Unit**	
	Christopher E. Lee	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 23 February 2007.
2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-48 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☒ Claim(s) 4,14,15,19,20,24,25,29 and 30 is/are allowed.
6)☒ Claim(s) 1-3,5-13,16-18,21-23,26-28 and 31-48 is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☐ All b)☐ Some * c)☐ None of:
1.☐ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 23rd of February 2007. Claims 1, 11, 21, and 31 have been amended; no claim has been canceled; and claims 45-48 have been newly added since the RCE Non-Final Office Action was mailed on 20th of September 2006. Currently, claims 1-48 are pending in this Application.

Claim Objections

2. Claims 3, 12, 13, 37, 39, 40, and 45-48 are objected to because of the following informalities:

In the claim 3, substitute "the bus protocol compliant signal" by --the master component bus protocol compliant signal-- in line 2.

In the claim 12, substitute "transition" in line 3 by --transit--.

In the claim 13, substitute "the first side component" in line 3 by --the first component--.

In the claim 37, substitute "the component associated with the first side" in lines 1-2 by --the first component associated with the first side-- and substitute "the component associated with the second side" in line 2 by --the second component associated with the second side--.

In the claims 39 and 40, substitute "the component associated with the second side" in line 2 by --the second component associated with the second side--, respectively, and substitute "the component associated with the first side" in line 3 by --the first component associated with the first side--, respectively.

In the claims 45 and 46, substitute "A method" in line 1 by --The method--, respectively.

In the claim 47, substitute "A bus bridge" in line 1 by --The bus bridge--.

In the claim 48, substitute "A computer-readable medium" in line 1 by --The computer readable recording medium--.

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 11-13, 16, 17, 21-23, 26, 27, 33, 35-37, 39-41, and 43-47 are rejected under 35 U.S.C. 102(b) as being anticipated by Evans et al. [US 6,253,250 B1; hereinafter Evans].

Referring to claim 1, Evans discloses a method for handling resets at a bus bridge (i.e., a method for bridging a plurality of buses and handling of an exception event, e.g., reset event, to provide bus isolation; See Abstract), the method comprising:

- providing a bus bridge (i.e., Bridge 213 of Fig. 2) coupling a master component (i.e., Memory 205 and Bus1 209 in Fig. 2) supporting a master component bus protocol (i.e., protocol for said Bus1, e.g., PCI bus protocol) to a slave component (i.e., Memory 207 and Bus2 211 in Fig. 2) supporting a slave component bus protocol (i.e., protocol for said Bus2, e.g., peripheral bus; See col. 2, lines 49-57);
- receiving a reset signal (i.e., Bus Reset Event) at the bus bridge (i.e., monitoring a bus exception signal line for the bus exception event in said Bus2; See col. 3, lines 4-6), the reset signal (i.e., said Bus Reset Event) associated with a reset of the slave component and not being associated with the master component (See col. 3, lines 30-32); and

- resetting said slave component and not resetting said master component (See col. 3, lines 34-37); and
- responding to a transaction from the master component to the slave component (i.e., transmission of data from said Bus1 to said Bus2) with a master component bus protocol compliant signal (i.e., signals for marking message as lost in transit in transmit descriptor, and for flushing any stale data in FIFO) after the reset signal is received (See Fig. 5B and col. 5, line 63 through col. 6, line 2),
    - wherein responding with the master component bus protocol compliant signal allows the master component to continue operating without violating said master component bus protocol while the slave component is being reset (e.g., a peripheral device on a bus is operating while an isolated reset on another device on another bus is performed; See col. 3, lines 38-51).

Referring to claim 2, Evans teaches

- the reset signal (i.e., Bus Reset Event; See col. 3, lines 34-37) is received at a bus bridge master interface (i.e., Bus2 Exception Monitor 251 in Fig. 2; See col. 3, lines 4-6).

Referring to claim 3, Evans teaches

- a bus bridge slave interface (i.e., DMA Engine1 235 of Fig. 2) responds with the master component bus protocol compliant signal (i.e., said DMA Engine1 is coupled and operating with Bus1 209 in compliance with a protocol for said Bus1 in Fig. 2, e.g., PCI bus; See Figs. 3 and 5B).

Referring to claim 11, Evans discloses a method for independently resetting a side of a bus bridge (i.e., a method for bridging a plurality of buses and handling of an exception event, e.g., reset event, to provide bus isolation in Bridge 213 of Fig. 2; See Abstract), the method comprising:

- receiving a reset signal (i.e., Bus Reset Event) on a first side of the bus bridge (i.e., Bus2 Exception Domain 217 of said Bridge in Fig. 2) and not on a second side of said bus bridge (i.e., Bus1 Exception Domain 215 of said Bridge in Fig. 2; See col. 3, lines 30-32);
- resetting a first component (i.e., Memory 207 and Bus2 211 in Fig. 2) associated with the first side of said bus bridge (i.e., said Bus2 Exception Domain) and not resetting a second side of said bus bridge (i.e., said Bus1 Exception Domain; See col. 3, lines 34-37);
- sending a signal (i.e., signals for marking message as lost in transit in transmit descriptor, and for flushing any stale data in FIFO) to a second component (i.e., Memory 205 and Bus2 209 in Fig. 2) associated with said second side of the bus bridge (i.e., said Bus1 Exception Domain) after receiving said reset signal (See Fig. 5B and col. 5, line 63 through col. 6, line 2), said signal being compliant with a bus protocol of said second side (in fact, said signals for marking message as lost in transit in transmit descriptor, and for flushing any stale data in FIFO are operating in said Bus1 Exception Domain anticipates that said signal is compliant with a protocol for Bus1 209 in Fig. 2); and
- continuing to operate said second component (i.e., said Memory 205 and Bus2 209 in Fig. 2) associated with said second side of the bus bridge (i.e., said Bus1 Exception Domain) while resetting said first component without violating said bus protocol of said second side (e.g., a peripheral device on a bus is operating while an isolated reset on another device on another bus is performed; See col. 3, lines 38-51),

  - wherein the first side (i.e., said Bus2 Exception Domain) corresponds to a first clock domain (in fact, a local clock domain of an independent local bus, e.g., a bus for Peripheral System 103 in Fig. 1) and the second side (i.e., said Bus1 Exception Domain) corresponds to a different second clock domain (in fact, a local clock domain of an independent local bus, e.g., a bus for Host System 101 in Fig. 1; See col. 1, lines 15-20).

Referring to claim 12, Evans teaches

- synchronizing the reset signal (i.e., Bus Reset Event; See col. 3, lines 34-37) to the second side of the bus bridge (i.e., Bus1 Exception Domain 215 of Bridge 213 in Fig. 2; See col. 2, lines 62-64; wherein, in fact that DMA Engine1 including Bus2 Exception Monitor to monitor for a bus exception event occurring in Bus2 implies that synchronizing the reset signal to the master component clock domain) such that a component associated with the second side (i.e., Memory 205 and Bus1 209 in Fig. 2) can transit to an idle state (i.e., stop data transmission and waiting until no bus exception in Bus2 exists in Step 507 in Fig. 5B).

Referring to claim 13, Evans teaches

- receiving the reset signal (i.e., Bus Reset Event; See col. 3, lines 34-37) at an interface (i.e., Bus2 Exception Monitor 251 in Fig. 2), the interface coupling the first side component to the bus bridge (i.e., said Bus2 Exception Monitor being coupled to Bus2 211 associated with Bus2 Exception Domain 217 to monitor a bus exception signal; See col. 3, lines 4-6).

Referring to claim 16, Evans teaches

- both the components (i.e., Memory 205, Bus1 209 and Memory 207, Bus2 211 in Fig. 2) are implemented in programmable logic (actually, both of said Memory are implemented in programmable logic, i.e., data being written on said Memories on System1 201 and System2 203 in Fig. 2; See col. 3, lines 14-26).

Referring to claim 17, Evans teaches

- one of the components (i.e., Memory 207 and Bus2 211 in Fig. 2) is implemented in hard logic (i.e., said Memory and Bus are hardware component; See col. 3, lines 14-26).

Referring to claim 21, Evans discloses a bus bridge (i.e., Bridge 213 of Fig. 2) for handling resets (i.e., for handling of an exception event, e.g., reset event, to provide bus isolation in said Bridge; See Abstract), the bus bridge comprising:

- a master interface reset input (i.e., means for generating bus exception event for Bus2 in Fig. 2; See col. 2, lines 62-64) arranged to receive a reset communication (i.e., bus exception signal, e.g., bus reset) and to generate a reset signal (i.e., Bus Reset Event) in order to reset a slave component (i.e., Memory 207 and Bus2 211 in Fig. 2; See col. 3, lines 34-37);
- a slave interface reset input (i.e., means for generating bus exception event for Bus1 in Fig. 2; See col. 2, lines 64-66) that does not generate any signal to reset a master component (i.e., Memory 205 and Bus1 209 in Fig. 2) while said slave component is being reset (e.g., a peripheral device on a bus is operating while an isolated reset on another device on another bus is performed; See col. 3, lines 38-51);
- a bus bridge master interface (i.e., DMA Engine2 237 of Fig. 2),

  - the bus bridge master interface (i.e., said DMA Engine2) coupled to said slave component (i.e., said Memory 207 and Bus2 211 in Fig. 2; See col. 2, lines 52-53 and 58-60),
  - the bus bridge master interface (i.e., said DMA Engine2) configured to receive said reset signal associated with said reset of the slave component (actually, said Bus Reset Event as a bus exception signal performs the operation of resetting said Memory 207 and Bus2 211 in Fig. 2) on a first side of the bus bridge (i.e., on Bus2 Exception Domain 217 of Fig. 2; See col. 3, lines 4-6 and 34-37),
    - wherein said first side of said bus bridge (i.e., said Bus2 Exception Domain) uses a first bus protocol (i.e., protocol for said Bus2, e.g., peripheral bus protocol; See col. 2, lines 49-57);
- a bus bridge slave interface (i.e., DMA Engine1 235 of Fig. 2),
  - the bus bridge slave interface (i.e., said DMA Engine1) coupled to said master component (i.e., said Memory 205 and Bus1 209 in Fig. 2; See col. 2, lines 51-52 and 57-58),
  - the bus bridge slave interface (i.e., said DMA Engine1) configured to interact with the master component (i.e., said Memory 205 and Bus1 209 in Fig. 2) on a second side of the bus bridge (i.e., on Bus1 Exception Domain 215 of Fig. 2) such that the slave component is reset while the master component continues operating without violating said first bus protocol (See col. 3, lines 38-51).

Referring to claim 22, Evans teaches

- the first side (i.e., Bus2 Exception Domain 217 of Fig. 2) corresponds to a first clock domain (in fact, a local clock domain of an independent local bus, e.g., a bus for

Peripheral System 103 in Fig. 1) and the second side (i.e., Bus1 Exception Domain 215 of Fig. 2) corresponds to a second clock domain (in fact, a local clock domain of an independent local bus, e.g., a bus for Host System 101 in Fig. 1),

- the first and second clock domains being different from each other (i.e., said two local clock domains are independent, and thus, the first and second clock domains are different from each other; See col. 1, lines 15-20).

Referring to claim 23, Evans teaches

- a synchronization logic (i.e., Bus2 Exception Monitor 251 of Fig. 2) for synchronizing the reset signal (i.e., Bus Reset Event; See col. 3, lines 34-37) with the second clock domain (i.e., a local clock domain of an independent local bus in Bus1 Exception Domain 215 of Bridge 213 in Fig. 2; See col. 2, lines 62-64; wherein, in fact that DMA Engine1 including Bus2 Exception Monitor to monitor for a bus exception event occurring in Bus2 implies that synchronizing the reset signal to the master component clock domain) such that the master component (i.e., Memory 205 and Bus1 209 in Fig. 2) and the bus bridge slave interface (i.e., DMA Engine1 235 of Fig. 2) transition to an idle state (i.e., stop data transmission and waiting until no bus exception in Bus2 exists in Step 507 in Fig. 5B).

Referring to claim 26, Evans teaches

- both the components (i.e., Memory 205, Bus1 209 and Memory 207, Bus2 211 in Fig. 2) are implemented in programmable logic (actually, both of said Memory are implemented in programmable logic, i.e., data being written on said Memories on System1 201 and System2 203 in Fig. 2; See col. 3, lines 14-26).

Referring to claim 27, Evans teaches

- one of the components (i.e., Memory 207 and Bus2 211 in Fig. 2) is implemented in hard logic (i.e., said Memory and Bus are hardware component; See col. 3, lines 14-26).

Referring to claim 33, Evans teaches

- either the master component (i.e., Memory 205 and Bus1 209 in Fig. 2) or the slave component (i.e., Memory 207 and Bus2 211 in Fig. 2) is implemented in programmable logic (actually, both of said Memory are implemented in programmable logic, i.e., data being written on said Memories) on a programmable device (i.e., on System1 201 or System2 203 in Fig. 2; See col. 3, lines 14-26).

Referring to claims 35 and 36, Evans teaches

- responding with a bus protocol compliant signal (i.e., signals for marking message as lost in transit in transmit descriptor, and for flushing any stale data in FIFO) allows the master component (i.e., Memory 205 and Bus1 209 in Fig. 2) to continue operating without stalling nor locking up while the slave component is being reset (See col. 3, lines 38-51 and col. 5, line 63 through col. 6, line 9).

Referring to claim 37, Evans teaches

- either the first component associated with the first side (i.e., Memory 207 and Bus2 211 in Fig. 2) or the second component with the second side (i.e., Memory 205 and Bus1 209 in Fig. 2) is implemented in programmable logic (actually, both of said Memory are implemented in programmable logic, i.e., data being written on said Memories) on a programmable device (i.e., on System1 201 or System2 203 in Fig. 2; See col. 3, lines 14-26).

Referring to claims 39 and 40, Evans teaches

- responding with a bus protocol compliant signal (i.e., signals for marking message as lost in transit in transmit descriptor, and for flushing any stale data in FIFO) allows the second component associated with the second side (i.e., Memory 205 and Bus1 209 in Fig. 2) to continue operating without stalling nor locking up while the first component associated with the first side is being reset (See col. 3, lines 38-51 and col. 5, line 63 through col. 6, line 9).

Referring to claim 41, Evans teaches

- the bus bridge (i.e., Bridge 213 of Fig. 2) is implemented on a programmable device (in fact, said Bridge is implemented on DMA Engines, which are programmable devices for the direct memory access operation; See col. 2 lines 42-48).

Referring to claims 43 and 44, Evans teaches

- the bus bridge slave interface (i.e., DMA Engine1 235 of Fig. 2) is configured to interact with the master component (i.e., said Memory 205 and Bus1 209 in Fig. 2) on the second side of the bus bridge (i.e., on Bus1 Exception Domain 215 of Fig. 2) such that the slave component is reset while the master component continues operating without stalling nor locking up while the slave component is being reset (See col. 3, lines 38-51 and col. 5, line 63 through col. 6, line 9).

Referring to claims 45-47, Evans teaches

- said received reset signal (i.e., Bus Reset Event; See col. 3, lines 34-37) is not associated with a system-wide reset (i.e., isolated reset signal; See col. 2, lines 35-39, and col. 3, lines 38-51).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 5-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans [US 6,253,250 B1] as applied to claims 1-3, 11-13, 16, 17, 21-23, 26, 27, 33, 35-37, 39-41, and 43-47 above, and further in view of Stewart et al. [US 6,687,773 B1; hereinafter Stewart].

Referring to claim 5, Evans discloses all the limitations of the claim 5, including the master component bus protocol (i.e., PCI bus protocol) operating in a master component clock domain (i.e., Bus1 Exception Domain 215 of Fig. 2; in fact, a local domain of an independent local bus, e.g., Host System 101 in Fig. 1; See col. 1, lines 15-20), except that does not teach the master component bus protocol is the AHB protocol.

Stewart discloses a bridge for coupling digital signal processor to on-chip bus as master (See Abstract), wherein

- a master component bus protocol (i.e., protocol for AHB Master on-chip Bus 30 in Fig. 1) is the AHB protocol (i.e., AMBA AHB protocol; See col. 4, lines 3-6 and 15-16) operating in a master component clock domain (i.e., AMBA AHB clock boundary; See col. 4, lines 40-43).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted buses for master component and slave component, as disclosed by Evans, by said AHB buses with said AMBA AHB protocol, as disclosed by Stewart, for the advantage of providing a high performance proprietary core integration (See Stewart, col. 2, lines 7-32).

Referring to claim 6, Evans, as modified by Stewart, teaches

- the slave component bus protocol (i.e., protocol for AHB Slave on-chip Bus 32 in Fig. 1; Stewart) is the AHB protocol (i.e., AMBA AHB protocol; See Stewart, col. 4, lines 3-6 and 15-16) operating in a slave component clock domain different from the master component clock domain (i.e., Bus2 Exception Domain 217 is an independent domain from Bus1 Exception Domain 215 in Fig. 2; thus, a clock in said Bus2 Exception Domain for Peripheral System is different from a clock in said Bus1 Exception Domain for Host System 101 in Figs. 1 and 2; Evans).

Referring to claim 7, Evans teaches

- the slave component bus protocol (i.e., protocol for Bus2 211 in Fig. 2, e.g., peripheral bus) is the PI protocol (i.e., the peripheral bus protocol; See col. 2, lines 49-57).
- Moreover, the claim merely recites the slave component bus protocol being the PI protocol without any patentable advantage in the specification. Therefore, the limitations of the PI protocol in the claim is not patentably significant since it at most relates to the kind of bus protocols consideration which is not ordinarily a matter of invention. *In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141*).

Referring to claim 8, Evans teaches

- synchronizing the reset signal (i.e., Bus Reset Event; See col. 3, lines 34-37) to the master component clock domain (i.e., Bus1 Exception Domain 215 of Fig. 2; See col. 2, lines 62-64; wherein, in fact that DMA Engine1 including Bus2 Exception Monitor to monitor for a bus exception event occurring in Bus2 implies that synchronizing the reset signal to the master component clock domain).

Referring to claim 9, Evans teaches

- setting the master component (i.e., Memory 205 and Bus1 209 in Fig. 2) to an idle state (i.e., stop data transmission and waiting until no bus exception in Bus2 exists in Step 507 in Fig. 5B).

Referring to claim 10, Evans teaches

- setting a bus bridge slave interface (i.e., DMA Engine1 235 of Fig. 2) in an idle state (i.e., stop data transmission and waiting until no bus exception in Bus2 exists in Step 507 in

Fig. 5B) while the slave component (i.e., Memory 207 and Bus2 211 in Fig. 2) is being reset (See col. 6, lines 2-9).

8. Claims 18 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans [US 6,253,250 B1] as applied to claims 1-3, 11-13, 16, 17, 21-23, 26, 27, 33, 35-37, 39-41, and 43-47 above, and further in view of Sweet [US 2005/0036577 A1].

Referring to claim 18, Evans discloses all the limitations of the claim 18, except that does not expressly teach receiving a synchronization signal by synchronization logic, the synchronization signal is a result of the reset signal; receiving a clock input by the synchronization logic, the clock input associated with the second clock domain; and outputting an initialization idle signal when the received clock input indicates that the second clock domain is running.

Sweet discloses a method for synchronizing resets in multi-clock frequency applications (See Abstract), wherein

- receiving a synchronization signal (i.e., Reset signal 106 of Fig. 4) by synchronization logic (i.e., Reset synchronizer 200 of Fig. 4), the synchronization signal (i.e., said Reset signal) is a result of a reset signal (i.e., a result of SW_Reset 403 or HW_Reset 405 in Fig. 4);
- receiving a clock input (i.e., Clock A 108 of Fig. 4) by the synchronization logic (i.e., said Reset synchronizer), the clock input (i.e., said Clock A) associated with a second clock domain (i.e., a function operating at said local Clock A; See paragraphs [0025] and [0026]); and
- outputting an initialization idle signal (i.e., Synchronized Reset 202 of Fig. 4) when the received clock input (i.e., said Clock A) indicates that the second clock domain is running

(i.e., said Clock A actively operating flip-flops 310 and 312 implies that the received clock input indicates that the second clock domain is running; in other words, said Synchronized Reset is not output if said Clock A is not operating, viz., the second clock domain is not properly running).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method for synchronizing resets, as disclosed by Sweet, in said method for independently resetting a side of a bus bridge, as disclosed by Evans, for the advantage of providing for synchronizing said reset signal with said received clock input in the second clock domain (i.e., a local clock signal; See Sweet, paragraph [0009]).

Referring to claim 28, Evans discloses all the limitations of the claim 28, except that does not expressly teach that the synchronization logic is configured for receiving a synchronization signal that is a result of the reset signal; for receiving a clock input that is associated with the second clock domain; and for outputting an initialization idle signal when the received clock input indicates that the second clock domain is running.

Sweet discloses a system for synchronizing resets in multi-clock frequency applications (See Abstract), wherein the synchronization logic (i.e., Reset synchronizer 200 of Fig. 4) is configured

- receiving a synchronization signal (i.e., Reset signal 106 of Fig. 4) that is a result of a reset signal (i.e., a result of SW_Reset 403 or HW_Reset 405 in Fig. 4);
- for receiving a clock input (i.e., Clock A 108 of Fig. 4) that is associated with a second clock domain (i.e., a function operating at said local Clock A; See paragraphs [0025] and [0026]); and

- for outputting an initialization idle signal (i.e., Synchronized Reset 202 of Fig. 4) when the received clock input (i.e., said Clock A) indicates that the second clock domain is running (i.e., said Clock A actively operating flip-flops 310 and 312 implies that the received clock input indicates that the second clock domain is running; in other words, said Synchronized Reset is not output if said Clock A is not operating, viz., the second clock domain is not properly running).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said system for synchronizing resets, as disclosed by Sweet, in said bus bridge, as disclosed by Evans, for the advantage of providing for synchronizing said reset signal with said received clock input in the second clock domain (i.e., a local clock signal; See Sweet, paragraph [0009]).

9. Claims 31, 32, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans [US 6,253,250 B1] and what was well known in the art, as exemplified by Luo et al. [US 6,265,885 B1; hereinafter Luo].

Referring to claims 31, 32, and 48, all of the claim limitations have already been discussed/addressed with respect to claims 1, 2, and 45, respectively, with the exception of a computer readable recording medium storing program instructions for handling said method of claim 1 (e.g., memory having a computer software program for handling said method in claim 1). The Examiner takes Official Notice that said method in the claim 1 being implemented in a program providing program instructions (i.e., a computer software program), and being stored in a computer readable recording medium (i.e., memory RAM, ROM, etc), is well known to one of ordinary skill in the art, as evidenced by Luo (See Claim 9, lines 2-4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said method of the claim 1, as disclosed by Evans, in said program providing program instructions (i.e., a computer software program), and being stored in a computer readable recording medium (i.e., memory RAM, ROM, etc), as disclosed by Luo, since it would have provided a better flexibility of implementing said method than a hardware implementation, such as an easy modification, etc.

10. Claims 34, 38, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans [US 6,253,250 B1] as applied to claims 1-3, 11-13, 16, 17, 21-23, 26, 27, 33, 35-37, 39-41, and 43-47 above, and further in view of Eaton et al. [US 6,552,410 B1; hereinafter Eaton].

Referring to claims 34, 38, and 42, Evans discloses all the limitations of the claims 34 and 38, respectively, except that does not teach the programmable device is selected from the group consisting of a PLD, a PLA, a PAL, a FPGA, and a CPLD.

Eaton discloses a programmable antifuse interfacing a programmable logic and a dedicated device (See Abstract), wherein

- a programmable device (i.e., integrated circuit 410 with PCI Core 414 and user circuitry 412 in Fig. 16) is a FPGA (See col. 12, lines 30-34).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used said programmable device, as disclosed by Eaton, for implementing said master and slave components, as disclosed by Evans, for the advantage of providing a user with the guaranteed functionality, ease-of-use, and high performance found in a dedicated device, as well as the configurability and flexibility found in programmable logic (See Eaton, col. 3, lines 54-59).

Allowable Subject Matter

11. Claims 4, 14, 15, 19, 20, 24, 25, 29, and 30 are allowed.

12. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 4, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that the bus protocol compliant signal is an AHB bus error signal.

With respect to claims 14 and 24, the claim limitations of the respective claims 14 and 24 are deemed allowable over the prior art of record as the prior art fails to teach or suggest that an alternating state handler being associated with the first side, wherein both the bus bridge master interface and the alternating state handler are configured for synchronously receiving the reset signal on the first side of the bus bridge.

The claim 15 is a dependent claim of the claim 14.

The claim 25 is a dependent claim of the claim 24.

With respect to claims 19 and 29, the claim limitations of the respective claims 19 and 29 are deemed allowable over the prior art of record as the prior art fails to teach or suggest that the bus bridge slave interface is configured for outputting a component idle signal to the master component in response to receiving the initialization idle signal, the component idle signal being used to trigger the master component to transition to an idle state.

The claim 20 is a dependent claim of the claim 19.

The claim 30 is a dependent claim of the claim 29.

Response to Arguments

13. Applicant's arguments with respect to claims 1, 11, 21, 31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Buckland et al. [US 5,815,647 A] disclose error recovery by isolation of peripheral components in a data processing system.

Manning [US 6,338,127 B1] discloses method and apparatus for resynchronizing plurality of clock signals used to latch restrictive digital signals, and memory device using same.

Hamilton et al. [US 7,165,172 B1] disclose facilitating cold reset and warm reset tasking in a computer system.

Cabezas et al. [US 6,662,320 B1] disclose method and apparatus for inhibiting an adapter bus error signal following a reset operation.

Bates [US 6,748,039 B1] discloses system and method for synchronizing a skip pattern and initializing a clock forwarding interface in a multiple-clock system.

Holm [US 6,087,867 A] discloses transaction control circuit for synchronizing transactions across asynchronous clock domains.

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on Monday through Friday, 9:30am - 6:00pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christopher E. Lee

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